

Intrinsic Non-Volatile Logic-in-Memory with STT-MRAM

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The invention relates to an electronic circuit comprising a plurality of 1T/1MTJ cells arranged in array and being selectable by word lines (WLs) and bit lines (BLs), wherein each 1T/1MTJ cell comprises an STT-operated magnetic tunnel junction (MTJ) and an access transistor.

REFERENCE:
M032/2012

DEVELOPMENT STATUS:
Extensive simulation studies

KEYWORDS:
Magnetic tunnel junction (MTJ), magnetoresistive random-access memory (MRAM), material implication (IMP), non-volatile logic-in-memory, spin-transfer torque (STT)

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COOPERATION OPTIONS:
■ License agreement
■ R&D cooperation

BACKGROUND

Reducing the power consumption and shortening the interconnection delay are two major targets for the next generation VLSIs. Therefore, several non-volatile logic-in-memory architectures, combining non-volatile memory and logic elements, have been proposed. However, these architectures require CMOS-based logic elements and sensing amplifiers to perform logic operations at each logic stage and to provide the next stage with appropriate signals as inputs. Furthermore, the logical computations are highly localized which limits the flexibility and the feasibility of performing logic operations between data stored in different memory elements. Therefore, in the state-of-the-art, large-scale integration of complex logic functions it is difficult or often even impossible using the non-volatile logic-in-memory concept due to the hard linking between different parts and the need for sensing amplifiers and intermediate circuitry.

TECHNOLOGY

In a logic mode, the proposed circuit simultaneously applies a selecting voltage V_s to a first word line (WL) and a pre-selecting voltage V_{ps} to a second WL to perform a logic operation called material implication (IMP). Based on the presented electronic circuit, it is possible to extend the functionality of a common STT-MRAM to include the capability of performing logic operations for which the need for sensing amplifiers and distributing logic devices over the memory block is eliminated. Any 1T/1MTJ cell in a bit line can be used to construct logic gates. Therefore, the logical computation is not localized and fewer elements are required to realize logical functions. Due to the non-local logic implementation, simple circuit structure, and being computationally complete, the disclosed logic-in-memory circuit is highly flexible and suited for large-scale non-volatile logic systems.

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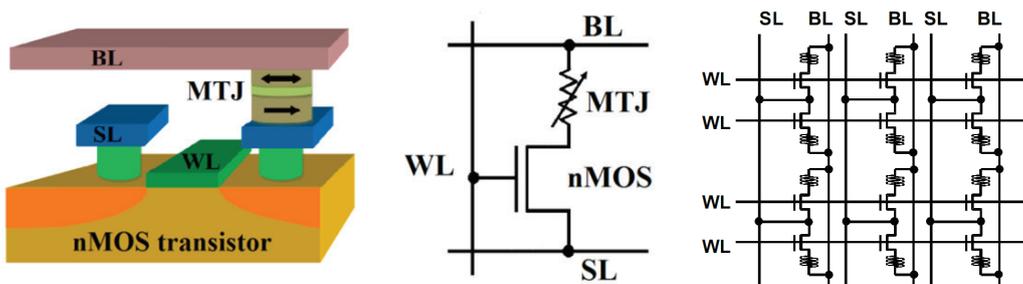


Fig. 1: The STT-MRAM exhibits the same circuit topology as DRAM, but instead of a capacitor an STT-operated magnetoresistive MTJ is exploited.

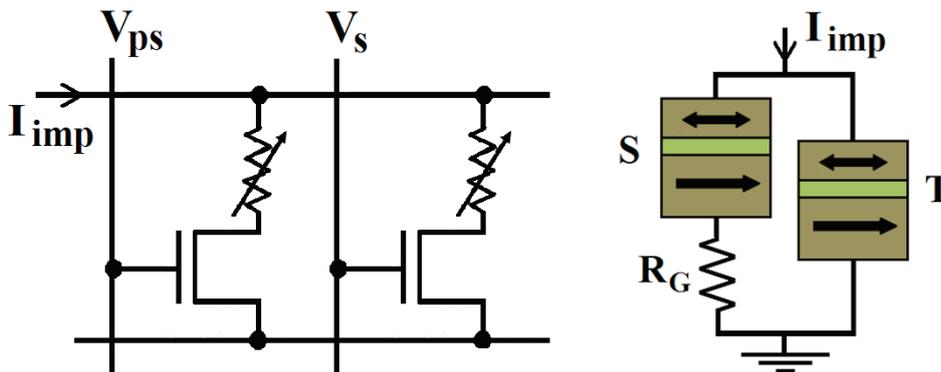


Fig. 2: The IMPLICATION operation can be realized by applying V_{ps} to the WL of the Source memory cell S, V_s to the WL of the Target memory cell T and current pulse I_{imp} .

BENEFITS

- High operation speed
- No standby power consumption
- Suitable for large scale integration
- Simple circuit structure (STT-MRAM)
- Less CMOS overhead than other MTJ/CMOS logic gates
- High flexibility

DEVELOPMENT STATUS

The proposed IMP gate and its feasibility has been thoroughly investigated via extensive simulation studies. The required STT-MRAM technology is mature and available as commercial off-the-shelf products. For the next step prototypes to proof the concept are required.

COOPERATION OPTIONS

The licensing of the invention, e.g. in exchange for research and development funding, is currently the preferred cooperation option, but we are open to discuss alternative offers.

APPLICATIONS

Due to the non-volatility, fast switching, high endurance, and radiation hardness of the employed magnetic tunnel junctions in combination with the high integration density capability of the 1T/1MTJ cells of the MRAM, a vast field of applications will benefit. For instance, field programmable gate arrays and their demanding applications in digital signal processing, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, radio astronomy, metal detection and many more will benefit from the merge of memory and logic gates within the MRAM and the possibility to easily reconfigure the dedicated RAM and logic gates depending on the task at hand as well as the increase in data safety due to the non-volatility and robustness of the MTJs. A further example is Internet of Things applications, since the invention allows zero standby power and a greatly simplified and flexible circuit design due to the dual use of the employed MRAM.

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